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The salient features of the book are as follows: • Hybrid Elements including topics like Memory organization, Binary representation of data, Computer arithmetic Software for parallel programming, tagged across some chapters through Quick Response (QR) Codes • Learning objectives

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tagged across chapters:

- Emphasis on parallelism, scalability and programmability aspects of computer architecture. It presents the analysis of scalability
- Issues related to instruction level parallelism, processor clock speed, and power consumption defined according to the recent developments in processor design
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- erial Bus, Real systems— IBM, Hitachi, Cray, Intel, UltraSparc, Blue Gene (from IBM), Cray XT series, XT5 and XMT, Fujitsu, DEC, MasPar, Tera, Stardent

Topical inclusions include:

- Pipelining hazards, data hazards and control hazards
- PCI Bus and PCI Express
- Interconnection networks and cluster computers
- MPI, openMP, PVM, Pthreads
- Multicore processors
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Computer architecture deals with the physical configuration, logical structure, formats, protocols, and

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operational sequences for processing data, controlling the configuration, and controlling the operations over a computer. It also encompasses word lengths, instruction codes, and the interrelationships among the main parts of a computer or group of computers. This two-volume set offers a comprehensive coverage of the field of computer organization and architecture.

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